THE ACCORDION IMAGER: MORE THAN JUST A CCD-SENSOR.

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Introduction.
A very high density frame transfer CCD is described which makes use of the accordion transport mechanism, and of a self-synchronisation algorithm. The last item can be applied because the accordion driving-circuitry itself provides synchronisation pulses for the imager.

The Accordion Transport.
To facilitate an interlaced operation of a frame transfer CCD-imager, the image area of the device consists mainly of four phases per cell. This pixel architecture implies that its minimum height equals 4 lithographic steps. For the image sensing function in itself two details would suffice: an area to store a charge packet and a barrier to separate that area from it's neighbours. This idea is put into practice by means of the accordion principle (ref 1), which is illustrated in Fig. 1. A cross-section through a vertical CCD-channel (1.a) is shown with the consecutive potential wells near the interface. At the end of the integration period (1.b), the frame shift starts. First the electrode at the extreme right is switched to the positive bias (1.c). Next the second gate is switched to zero (1.d) . Now the last two charge packets are separated by two zero-biased electrodes and the next electrode can be switched positive (1.e). This transport sequence continues and each charge packet starts to be transported once it is separated by two zero-biased electrodes from the previous one. This mode of transportation is achieved by addressing the CCD-electrodes through a two-phase, on-chip shift register (Fig. 2), realised in dynamic CMOS-logic.

As already depicted in Fig. 2, a complete frame transfer CCD contains two accordions: an image and a storage one, both synchronised but with the possibility to drive them seperately. The transfer of the charge-packets by means of an accordion transport sequence from the image section to the storage region is depicted in Fig.3. Black rectangles represent potential wells with information, open rectangles represent potential barriers which are needed to seperate the different charge-packets.

Synchronisation demands.
Each frame transfer CCD needs synchronisation pulses to shift the charge packets from the image to the storage section and from the storage area to the output register. For the accordion CCD, a few extra synchronisation pulses are needed because each stretching of the device has to be followed by a folding up of the accordion. Consequently, start pulses are required just to initialise:

1 the stretching of the image accordion,
2 the closing of the storage accordion,
3 the closing of the image accordion,
4 the stretching of the storage accordion.

Most of the counting part of the synchronisation electronics was built in twofold off-chip, because of the interlaced operation of the device.

Self Synchronising Accordion.
In the new device, the above-mentioned four time points are translated in:

1 the end of the integration period,
2 the end of the stretching of the image accordion,
3 the end of the closing of the storage accordion,
4 the end of the closing of the image accordion.

The last three "end points" can be detected by means of a small electronic circuit (about 20 gates) which is built on-chip in CMOS-logic. The detection itself is performed just by looking at the logical value of the last stage ($LS_i(t)$ for the image section, $LS_s(t)$ for the storage section) of the driving shift register. Two sequential values of this digital information tell everything about the status of the accordion(s): completely opened or completely closed. The flow-chart of the detection algorithm is depicted in Fig. 4a.

As described in ref. 1, the movement of the accordion(s) is determined by the input(s) IM and ST of the driving shift registers (see also Fig. 2). A constant value on ST (IM) closes the storage (image) accordion, while pulsing ST (IM) opens the accordion and forces the device in a four-phase transporting mode. The appropriate logical levels on the inputs ST and IM are also generated by the detection circuit which is implemented on-chip. The corresponding values for ST and IM are also shown in Fig. 4b.

Conclusion.
The accordion imager is more than just a CCD-imager: thanks to the digital drive-circuitry it has inherently its own synchronisation logic on-chip. This may prove the first step towards a self contained single chip camera

Acknowledgement.
The authors are indebted to M.G. Collet for his contributions and encouragement. Also thanks to D. de Gree and C.A.M. Jaspers for their fruitful discussions.

References.
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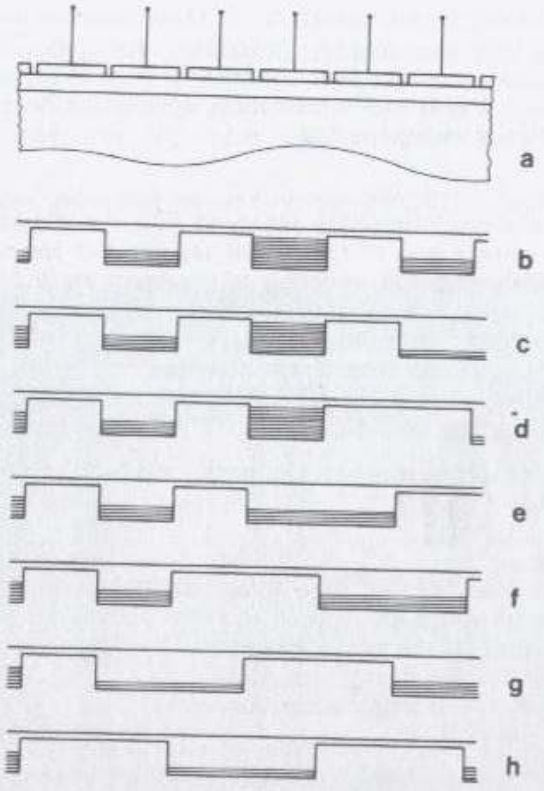

Figure 1.
The accordion read-out mechanism : going from a two-phase integrating system towards a classical four-phase transporting device.

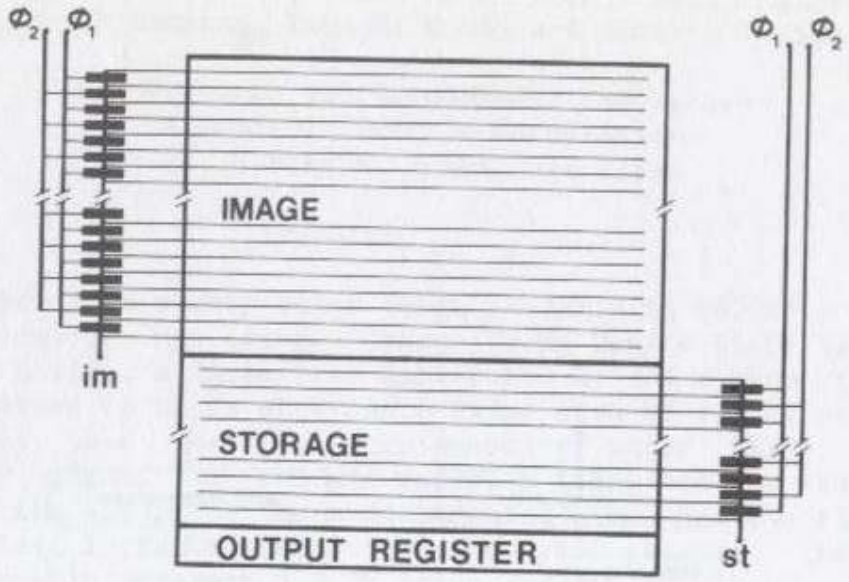

Figure 2.
Realization of the accordion driving circuitry by means of two digital shift-register.

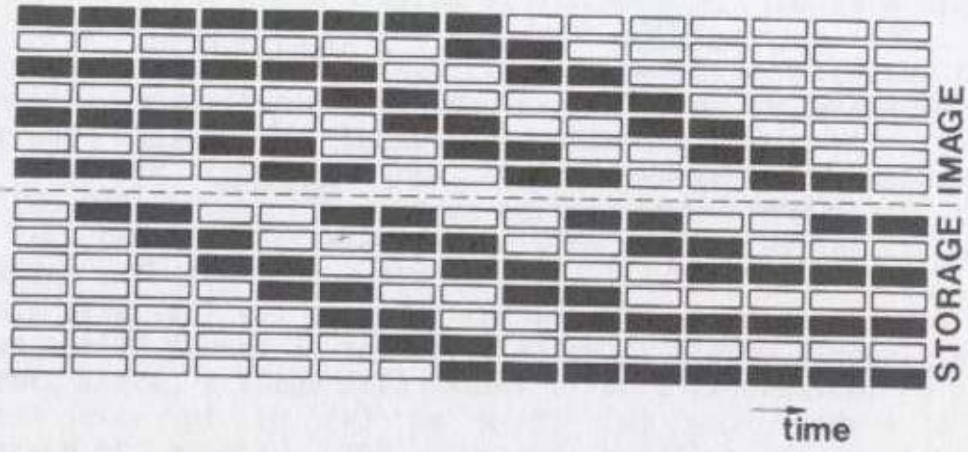

Figure 3.
Opening of the image accordion, run over into the storage accordion, and closing of the latter.

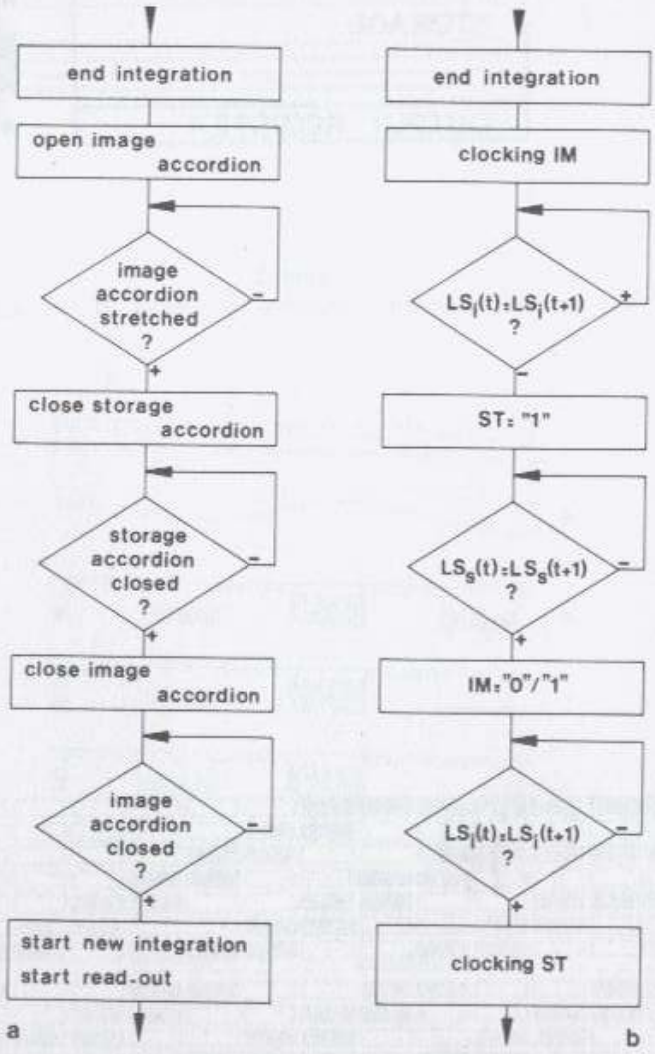

Figure 4.
Flow-chart of the synchronisation-algorithm, which is implemented on the accordion CCD-chip.