High Density Frame Transfer Image Sensors with Vertical Anti-Blooming

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Abstract

In Frame Transfer (FT) imagers all of the imaging area is sensitive to light. If one succeeds in defining pixels of only two photolithographic details (the pixel itself and the separation to its neighbours) FT sensors would allow maximum resolution as well as maximum sensitivity. This paper shows how the use of multiple horizontal read-out registers, vertical anti-blooming and the "accordion principle" allows us to achieve this goal. These concepts are illustrated with a 7.5 mm image diagonal colour image sensor and a 5.2 mm diagonal black and white imager, both with two interlaced fields of 180.000 pixels each.

Introduction

Ideally, an image sensor should use all of the incoming light and have as many pixels as prescribed by the application. Frame Transfer imagers[1] consist of an image area, a storage area and a read-out register (fig. 1). Image and storage area contain a large number of

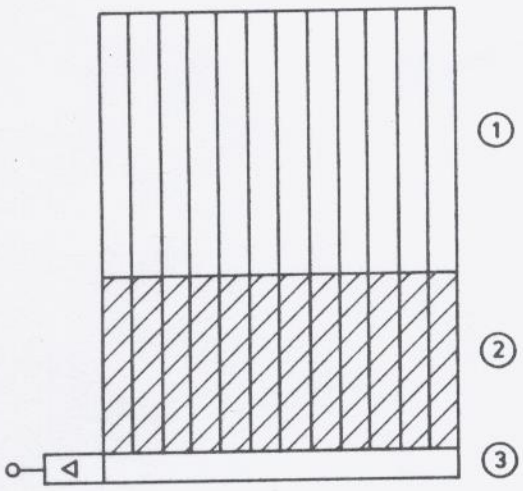

Figure 1: Frame Transfer sensor. 1, image area; 2 storage area; 3 read-out register

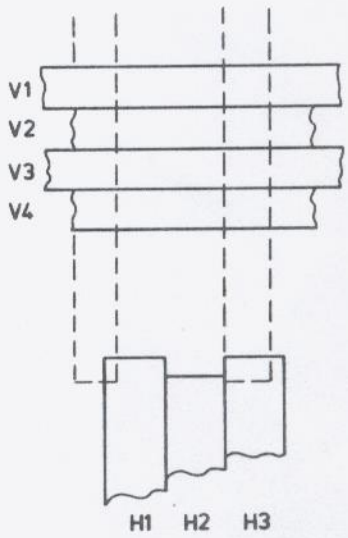

Figure 2: Image area unit cell and read-out register cell.

parallel CCD registers. The number of CCD cells in the image area equals that in the storage area. Light projected on the image area creates electron charge packets in each CCD cell. After one integration period the complete charge distribution is transferred quickly from the image to the storage section, which is shielded against light. During the next integration period the information is transferred one line at a time to the horizontal read-out register and read out through the output amplifier. At the same time a new charge distribution is built up in the image area.
Note that the image area basically uses all of the incoming light. In state of the art devices reflection losses and absorption in CCD gate electrodes occur, but the basic sensor mechanism does not preclude 100% light usage.
Figure 2 shows a unit cell in the image area as well as a unit cell of the horizontal read-out register. In the image area four phase electrodes per cell are often used to facilitate interlaced operation[2]. In the read-out registers a minimum of three electrodes is needed

per unit cell. Since the width of the pixel has to accommodate the length of one read-out register cell, the minimum pixel size equals four by three lithographic details. For the image sensing function in itself two-by-two details would suffice: an area to store a charge packet and a barrier to separate that area from its neighbours. The following chapters will show such a minimum size cell to be quite feasible.

Multiple Read-out Registers

Figure 3 shows how the use of three read-out registers in parallel allows the horizontal pitch of the pixels to be reduced to a minimum[3]. At the top of the figure three vertical CCD channels of the storage section debouch into the first horizontal read-out register. The channels of the three parallel read out registers are connected by openings in the channel stop diffusions. The potential in these openings is governed by transfer gates (TG 1, 2). The read-out registers have common phase electrodes (ø 1,2,3). By applying the proper sequence of pulses to these electrodes and to the transfer gates the charge packets at A, B and C are transferred to positions A', B' and C' respectively. These transfers take place during the line blanking. During the active video line time the three horizontal registers are read out in parallel. Using this construction we need just one horizontal phase electrode per vertical CCD channel and the read-out register no longer limits the packing density of the image area.
Instead of three one may use two read-out registers in parallel[4]. With four-phase

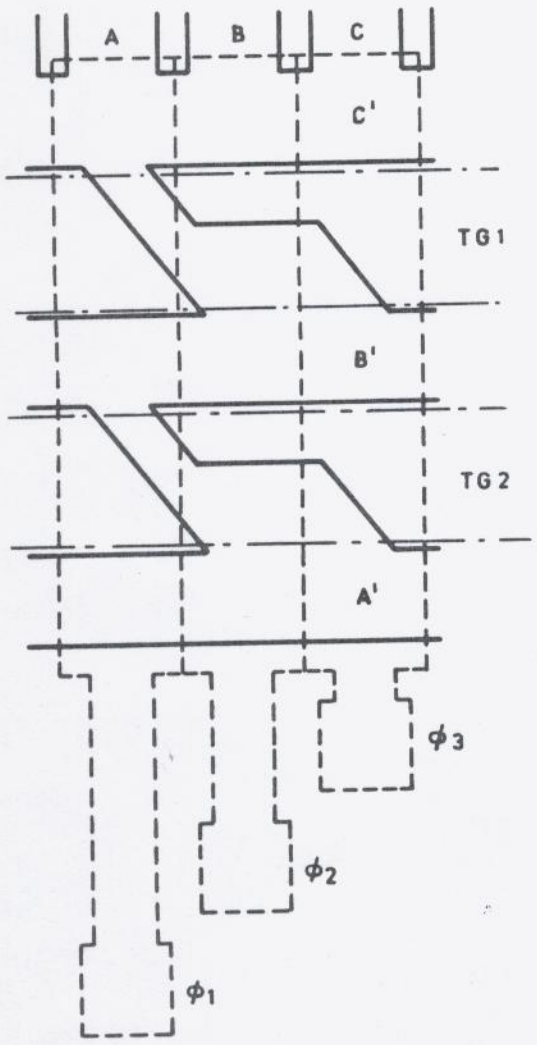

Figure 3: Triple read-out register. Solid lines: channel-stop boundaries, dashed and dot-dashed lines poly silicon electrodes

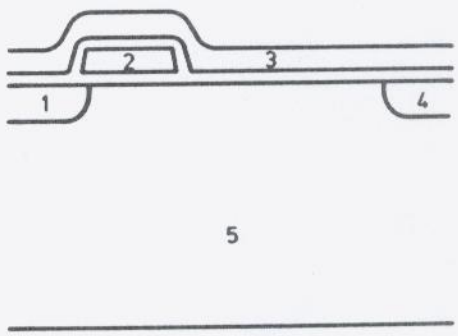

Figure 4: Cross-section of a pixel with blooming control, 1:n^+-overflow drain; 2: control gate; 3: CCD electrode; 4: channel stop; 5: p substrate

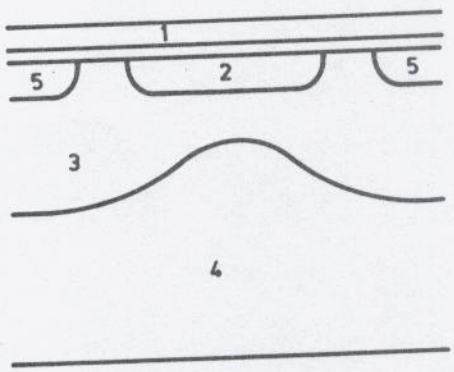

Figure 5: Cross-section of an FT pixel with VAB. 1: CCD electrode; 2: n-buried channel; 3: p-well; 4: n-substrate; 5: p^+ channel stop

clocking for these registers two horizontal phase electrodes per vertical CCD are sufficient and again the cell size of the horizontal register does not limit the pixel width. Which of these solutions is to be chosen depends on the application of the image sensor. For colour imaging, using vertical stripe filters in three colours (e.g. yellow, green and cyan) a triple read-out register is attractive because the colour signals can be transported through separate channels. When quadruple stripe filters (f.i. red, green, blue, green) are used a double read-out register is preferable: one for green, the other for blue and red.

Vertical Anti-Blooming

In many applications the dynamic range in the scene is larger than the dynamic range of the imager. Highlights will cause more electrons to be generated than can be stored locally. The excess electrons tend to spill over to neighbouring pixels along the same CCD channel. The resulting white vertical lines on the displayed image are unacceptable. To prevent this "blooming" one can use overflow drains and overflow control gates[5] as shown in figure 4. When the voltage on the control gate is more positive than the voltage on the most negative of the CCD electrodes, excess electrons will spill over to the n^+ drain and blooming is prevented. Because this solution requires two additional details per pixel width it limits resolution.
In Charge Injection Devices[6], XY addressed[7] and Inter Line transfer[8] imagers, ways have been found to remove excess electrons to the substrate, without sacrificing chip area. It is possible to achieve Vertical Anti-Blooming (VAB) in FT imagers as well[9]. Figure 5 shows a cross-section of a FT pixel with this mode of blooming control. The n-type buried channel CCD is formed in a p-well on an n-type substrate. The dopant distribution in this cell has to be optimised with respect to many performance criteria of the imager:

a. excess electrons have to spill over to the substrate through the thinner part of the p-well before flowing into neighbouring pixels.

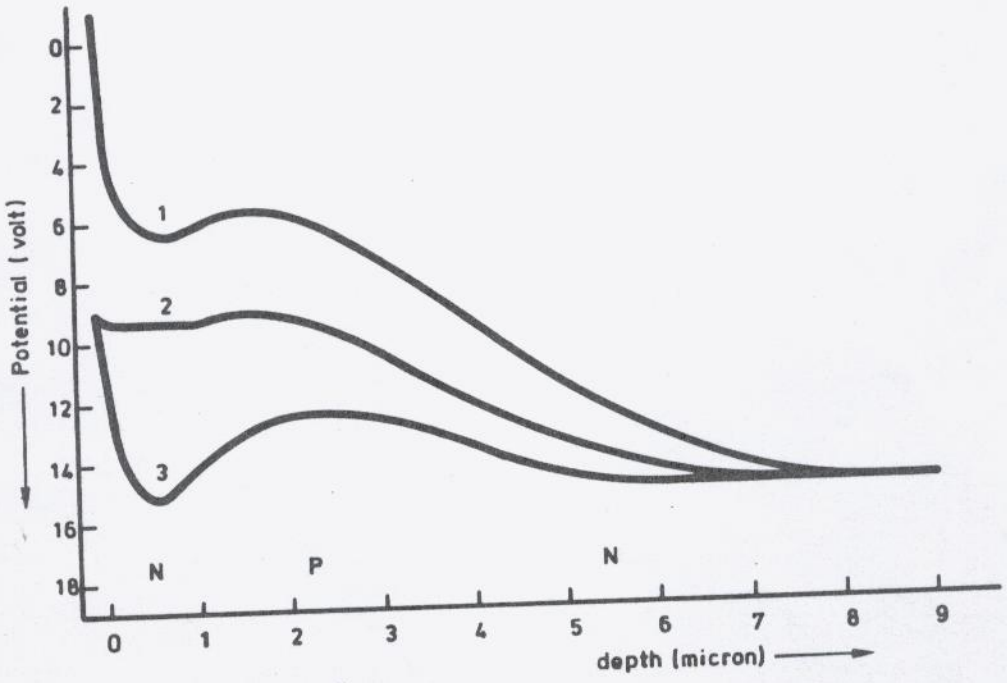

Figure 6: Potential profiles for blooming control. 1: under the barrier electrode; 2: under the integrating electrode with maximum charge packet and (3) without charge.

b. the average depth of the p-well has to be sufficient to yield high sensitivity for green and shorter wavelength red light. (Of course all electrons generated in the n-substrate by longer wavelengths are lost.)
c. the maximum charge packet that can be stored in a pixel should provide a large dynamic range.
d. the transfer speed of the horizontal read-out registers (preferably to be realised with the same implantations and anneals) should be sufficient.
e. punch-through from the CCD channel to the substrate or vice versa should be prevented at all operating voltages.
f. operating voltages should be low.

Reference 9 describes the methods used to model the dopant profiles and the resulting potential distributions. As an example figure 6 gives the potential profiles used in an FT sensor with 588 lines (two interlaced frames of 294 lines each) and 604 pixels per line on an image area of 4.5x6.0 mm^2. Triple read-out registers are used since the sensor has been designed for use in a single sensor colour camera with on-chip cyan, green and yellow colour filters.
Figure 7 shows a resolution chart taken with this sensor and table I gives some parameters for performance in a black and white camera.

Table I. Parameters of 355.000 pixel FT sensor.

Design rule	3.6 µm
Pixel	15.6x10.0 μm^2
Image area	4.5x 6.0 mm^2
Chip area	66 mm^2
Horizontal resolution	400 lines
Sensor illumination for S/N= 40 dB	2 lux
Overexposure	100 x
Maximum charge/pixel	10^5 electrons
Package: DIL	24 pins

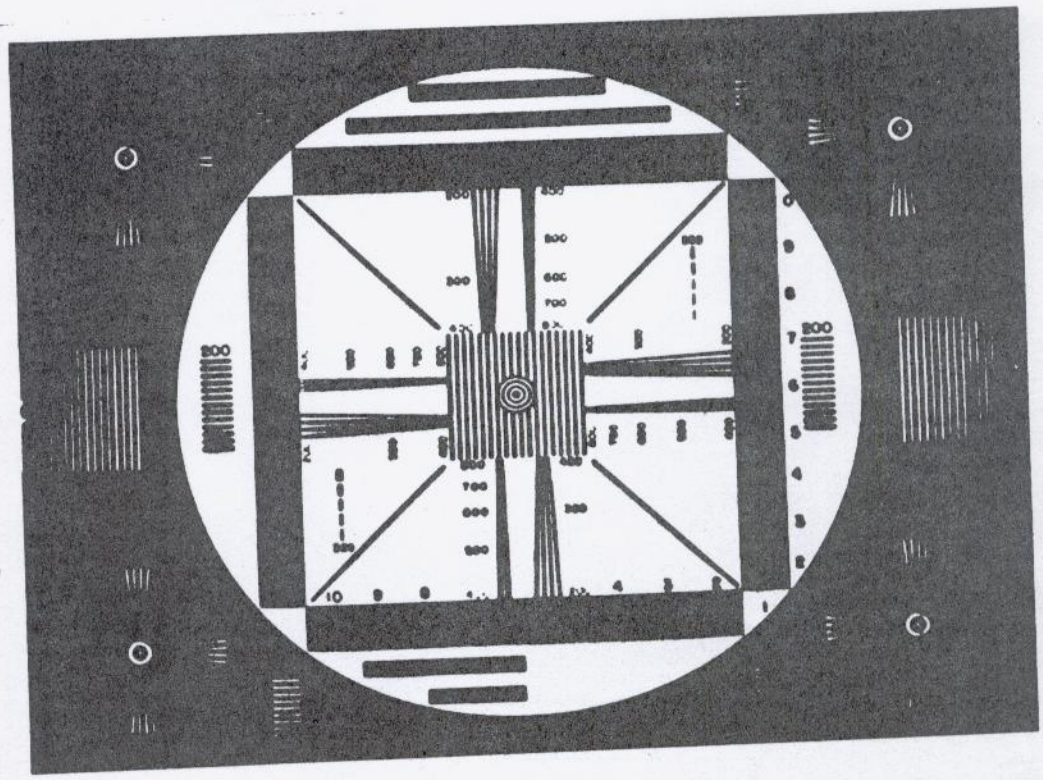

Figure 7: Resolution chart taken with 355000 pixel FT sensor.

The Accordion Principle

The previous chapters have shown it is possible to achieve minimum pixels widths in FT sensors. The accordion principle allows to realise minimum pixel heights as well[10].
Figure 8 shows a cross-section through one of the vertical CCD channels of such an imager;

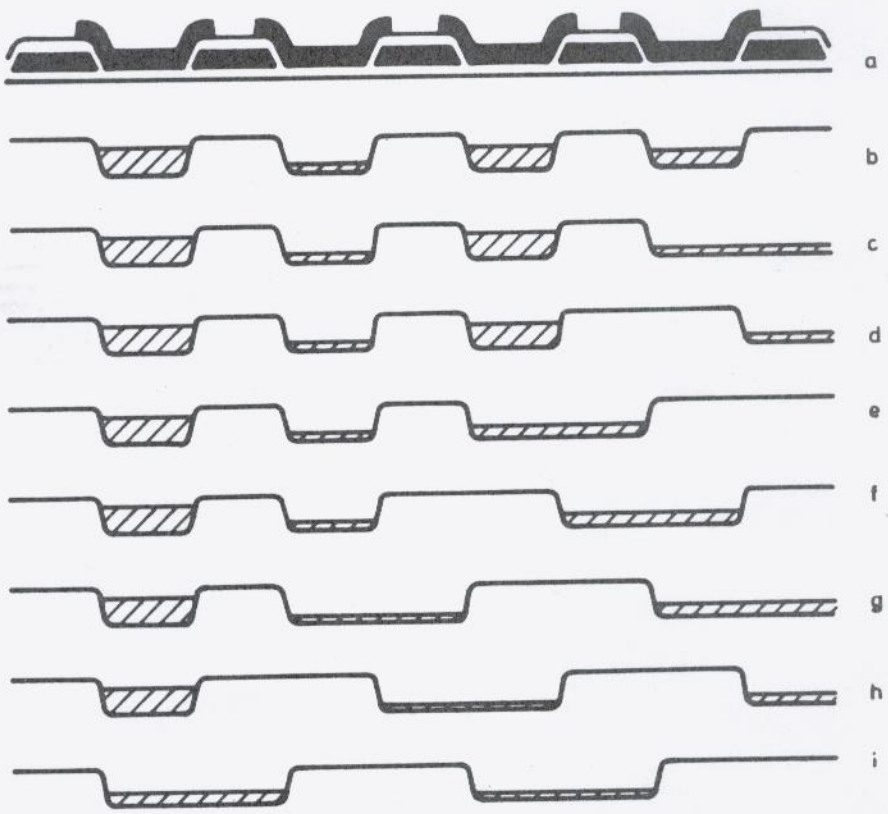

Figure 8: the accordion mechanism;
a: cross-section along the channel,
b-i; potential positions at consecutive moments in time

below the cross-section the position of the potential wells at consecutive moments in time is given. During the integration period half the CCD electrodes are at positive, the other half at zero bias. Hence one charge packet is integrated under a set of two electrodes (fig. 8b), in contrast to the classical FT pixel (fig. 2) where four electrodes were used. At the end of the integration period the frame shift starts. First the electrode separating the image from the storage section (at the extreme right in fig. 8c) is switched to positive bias. Next the last electrode of the image section is switched to zero (fig. 8d). Now the last two charge packets are separated by two zero-biased electrodes and the next but last electrode of the image area can be switched positive (fig. 8e). This process continues and each charge packet starts to be transported once it is separated by two zero-biased electrodes from the previous one.
This mode of transportation is achieved by addressing the CCD electrodes through a two-phase, on-chip shift register (fig. 9), realised in dynamic CMOS logic to limit power dissipation.
When the input (S) of the shift register is kept constant, clocking of the shift register

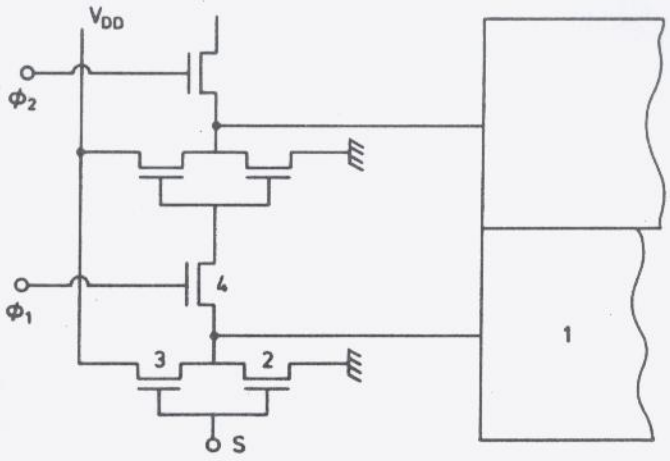

Figure 9: Two-phase shift register addressing of CCD electrodes; 1: CCD electrodes, 2: n-channel and (3) p-channel MOST of inverter stage, 4: n-channel transfer MOST, S: input signal, ϕ_1 and ϕ_2: clock pulses, V_{DD}: positive supply voltage

will lead to a stationary state where the outputs of the register will be alternately positive and zero. This is the integrating mode, interlacing is achieved by taking S zero during one frame and positive during the next. When S is clocked at half the frequency of ϕ_1, and ϕ_2 a four-phase clocking mode starts to propagate along the CCD electrodes as illustrated in figure 10.

	S	ϕ_1	ϕ_2	CCD electrodes					
				1	2	3	4	5	6
t_1	0	0	+	+	0	+	0	+	0
t_2	+	+	0	0	0	+	0	+	0
t_3	+	0	+	0	+	+	0	+	0
t_4	0	+	0	+	+	0	0	+	0
t_5	0	0	+	+	0	0	+	+	0
t_6	+	+	0	0	0	+	+	0	0

Figure 10: Timing sequence at the onset of accordion clocking.

Both figure 8 and 10 show how the charge packets are gradually stretched from a most densely packed distribution during integration into the more spacious distribution during transportation. This rippling movement has suggested the name accordion imager.
In the storage section the same mechanism is used. At the end of an integration period the storage section is empty and the four-phase transportation mode has propagated to the top of the storage section. Then read out of the image section starts as described above. When the transportation mode has propagated to the top of the image section the bottom line of the image has just reached the bottom line of the storage section. From that moment on the input signal of the storage section shift register is kept constant. Now the stationary, charge storage mode propagates from the bottom upwards through the storage section. At the end of the frame shift all charge packets are densely packed in the storage section, the image section is empty but still in the transportation mode. Then the input signal of the image section shift-register is kept constant again and the integration mode propagates to the top of the image section. Read out of the storage section into the horizontal read-out register then starts, similar to the read-out of the image section.

An experimental imager with accordion clocking in image and storage section, with triple read-out registers and vertical anti-blooming has been realised. It has the same number of pixels as the FT imager of table I, but uses only 38 mm^2. Table II shows how this area is distributed over shift registers, image section, storage section and periphery (bond pads etc.). Table III presents some of this sensor's characteristics. A picture of a test chart taken with this sensor is not included because it is identical with the one taken with the classical FT sensor (fig. 7).

Table II. Accordion sensor, sensor area usage

Image section	36%
Storage section	29%
Shift registers	17%
Read-out registers	3%
Periphery	34%

Table III. Characteristics of accordion imager

Design rule	3 µm
Pixel size	11x7 μm^2
Image area	3.2x4.2 mm^2
Chip area	38 mm^2
Hor-resolution	400 lines
Sensor illumination for S/N = 40 dB	4 lux
Overexposure protection	100 x
Maximum charge	10^5 electrons
Package DIL	18 pins

The main difference between tables I and III, apart from geometry, is the illumination intensity needed on the sensor to achieve a 40 dB signal to noise ratio. Since the pixels are smaller more photons per unit area are needed to generate the same number of electrons per pixel. This difference can be partly compensated by using a lens with larger aperture, since the focal depth of the camera remains constant when the product of lens opening and image diagonal remains constant.

Conclusions

In solid state imaging the smallest pixel dimensions conceivable equal two by two photolithographic details. Using the Frame Transfer organisation together with multiple read-out registers, vertical anti-blooming and the accordion principle these minimum dimensions can be realised. Using transparent electrodes and anti-reflection coatings it should become possible to achieve close to 100% quantum efficiency as well.

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References

1. Thompsett, M.F.; Amelio, G.F.; Bertram, W.J.; Buckley, R.R.; McNamara, W.J.; Mikkelson, J.C. and Sealer, D.A. IEEE Trans. on Electron Devices ED-18, 992 (1971).

2. Sequin, C.H. IEEE Trans. on Electron Devices ED-20, 535 (1973).

3. Beck, G.A.; Collet, M.G.; Van Gils, J.A.A.; Klinkhamer, A.J.; Peek, H.L.; Ruis, W.N.J.; van Santen, J.G.; Smit, T.F.; Vandormael, G.T;J. Digest of The 14th Conference (1982 International) on Solid State Devices, Tokyo, Japanese J. of Applied Phys. 1983. Supplement 22-1, p. 109.

4. Tredwell, T.J.; Lee, T.H.; Burkey, B.C.; Kelly, T.M.; Rhosla, R.P.; Losee, D.L.; Lo, F.C.; Nielsen, R.L.; McColgin, W.C. Digest of the IEDM 1983, Washington, p. 492.

5. Seguin, C.H. Bell Syst. Tech. Jour. 51, 1923 (1972).

6. Michon, G.J.; Burke, H.K. ISSCC, Philadelphia 1974, Digest p. 26.

7. Koike, N.; Takemoto, I.; Sato, K.; Matsumaru, H.; Ashikawa, M.; Kubo, M. ISSCC, Philadelphia, 1979, Digest p. 192.

8. Ishihara, Y.; Oda, E.; Tanigawa, H.; Teranishi, N.; Takenchi, E.; Akiyama, I.; Arai, K.; Nishimura, M.; Kamata, T. ISSCC San Fransisco 1982, Digest p. 168.

9. Van de Steeg, M.J.H.; Peek, H.L.; Bakker, J.G.C.; Pals, J.A.; Dillen, B.G.M.H.; Oppers, J.M.A.M. to be published in IEEE Trans. on Electron Devices ED-32, 1985.

10. Theuwissen, A.J.P.; Weijtens, C.H.L.; Esser, L.J.M.; Cox, J.N.G.; Duyvelaar, H.T.A.R.; Keur, W.C. IEDM San Francisco 1984, Digest p. 40.